

Wider power copper - measured changes

Separate R15 revision. Component locations, signal routes, vias, board size and six-layer stack are retained.

437 existing power/ground track segments widened across 12 nets. The following ranges refer only to changed segments; local pad necks and sensitive return paths are classified separately.

Net	Changed segments	R14 widths (mm)	R15 widths (mm)
BUCK_3V3	34	0.3 - 3	0.4 - 6.3
DGND	149	0.2 - 1	0.25 - 8
LDO_3V3	8	0.2 - 0.5	0.3 - 1
USBJTAG_3V3	92	0.2 - 0.35	0.25 - 2
USBJTAG_VBUS_C	19	0.2 - 0.4	0.25 - 1
USBJTAG_VCCA	2	0.2 - 0.2	0.3 - 0.3
USBJTAG_VCORE	2	0.2 - 0.2	0.25 - 0.25
USBJTAG_VPHY	13	0.2 - 0.25	0.25 - 1
USBJTAG_VPLL	8	0.2 - 0.2	0.25 - 0.65
USBJTAG_VREGIN	17	0.2 - 0.3	0.25 - 1
VDCIN	33	0.2 - 2.5	0.5 - 4.2
XEM_1V8	60	0.2 - 0.8	0.35 - 2

Widths are clearance- and function-limited on the existing routes. This is not a claim of an absolute mathematical maximum or verified ampacity. Existing shared outer ground/supply paths are checked separately after refill.

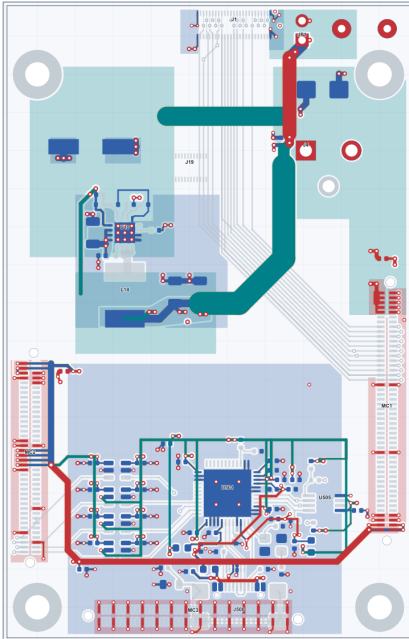
Whole-board width-change context

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

Whole-board width-change context
Example: BUCK_3V3 In3.Cu 3 → 4.8 mm



10 mm · exact same scale
B.Cu In3.Cu F.Cu changed width

Changed copper widths: 0.2–3 mm · 437 native sections

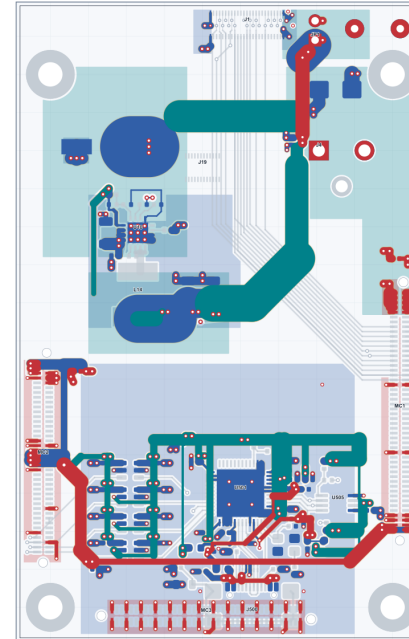
Selected-net vias in window: 253 · changed tracks: 437 · top view; B.Cu not mirrored

Nets: BUCK_3V3, DGND, LDO_3V3, USBJTAG_3V3, USBJTAG_VBUS_C, USBJTAG_VCCA, USBJTAG_VCORE, USBJTAG_VPHY, USBJTAG_...

AFTER - R15

AFTER · R15

Whole-board width-change context
Example: BUCK_3V3 In3.Cu 3 → 4.8 mm



10 mm · exact same scale
B.Cu In3.Cu F.Cu changed width

Changed copper widths: 0.25–8 mm · 437 native sections

Selected-net vias in window: 253 · changed tracks: 437 · top view; B.Cu not mirrored

Nets: BUCK_3V3, DGND, LDO_3V3, USBJTAG_3V3, USBJTAG_VBUS_C, USBJTAG_VCCA, USBJTAG_VCORE, USBJTAG_VPHY, USBJTAG_...

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Orientation and coverage map; local comparisons provide readable detail for each affected region.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.

Parts: J1, J19, JP1, J4, U10, L14, MC1, MC2, MC3, U501, U505, J500 | Layers: B.Cu, In3.Cu, F.Cu

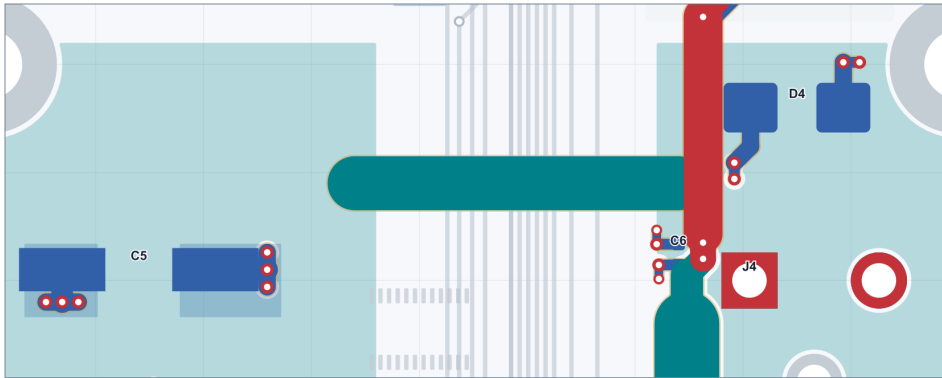
12 V input, bulk capacitor and protection

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

12 V input, bulk capacitor and protection
Example: VDCIN In3.Cu 2.5 → 4.2 mm

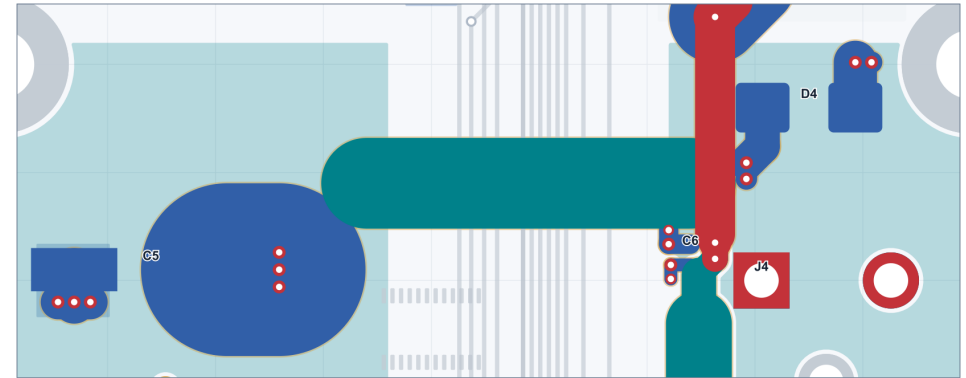


10 mm · exact same scale
— B.Cu — In3.Cu — F.Cu — changed width
Changed copper widths: 0.4–3 mm · 23 native sections
Selected-net vias in window: 17 · changed tracks: 23 · top view; B.Cu not mirrored
Nets: BUCK_3V3, DGND, VDCIN

AFTER - R15

AFTER · R15

12 V input, bulk capacitor and protection
Example: VDCIN In3.Cu 2.5 → 4.2 mm



10 mm · exact same scale
— B.Cu — In3.Cu — F.Cu — changed width
Changed copper widths: 0.6–8 mm · 23 native sections
Selected-net vias in window: 17 · changed tracks: 23 · top view; B.Cu not mirrored
Nets: BUCK_3V3, DGND, VDCIN

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: C5, C6, D4, J4 | Layers: B.Cu, In3.Cu, F.Cu

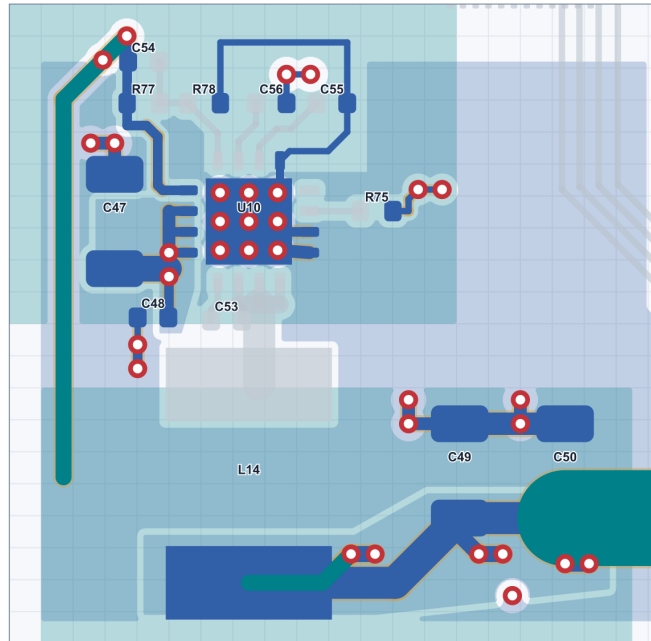
Converter input, output and bypass copper

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

Converter input, output and bypass copper
Example: BUCK_3V3 B.Cu 1 → 3.8 mm

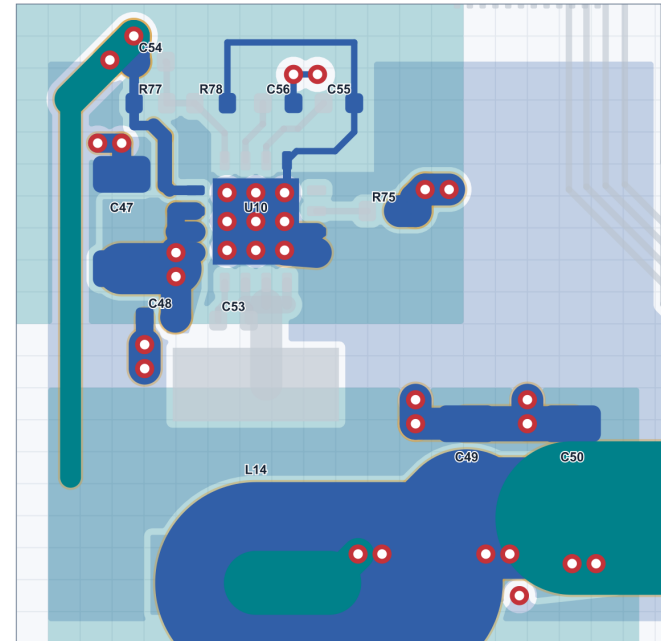


5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.2, 0.3, 0.4, 0.5, 0.7, 0.8, 1, 3 mm · 46 native sections
Selected-net vias in window: 32 · changed tracks: 46 · top view; B.Cu not mirrored
Nets: BUCK_3V3, DGND, VDCIN

AFTER - R15

AFTER · R15

Converter input, output and bypass copper
Example: BUCK_3V3 B.Cu 1 → 3.8 mm



5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.4–6.3 mm · 46 native sections
Selected-net vias in window: 32 · changed tracks: 46 · top view; B.Cu not mirrored
Nets: BUCK_3V3, DGND, VDCIN

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: U10, L14, C47, C48, C49, C50, C53, C54, C55, C56, R75, R77, R78 | Layers: B.Cu, In3.Cu, F.Cu

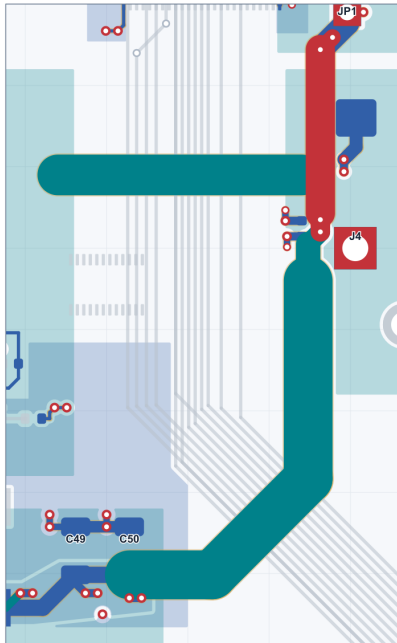
Main 3.3 V transfer and jumper feed

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

Main 3.3 V transfer and jumper feed
Example: BUCK_3V3 In3.Cu 3 → 4.8 mm



5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width

Changed copper widths: 0.2–3 mm · 47 native sections

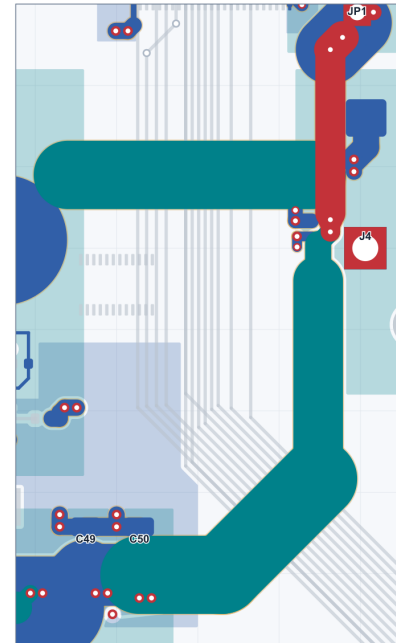
Selected-net vias in window: 27 · changed tracks: 47 · top view; B.Cu not mirrored

Nets: BUCK_3V3, DGND, LDO_3V3, VDCIN

AFTER - R15

AFTER · R15

Main 3.3 V transfer and jumper feed
Example: BUCK_3V3 In3.Cu 3 → 4.8 mm



5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width

Changed copper widths: 0.35–6.3 mm · 47 native sections

Selected-net vias in window: 27 · changed tracks: 47 · top view; B.Cu not mirrored

Nets: BUCK_3V3, DGND, LDO_3V3, VDCIN

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: C49, C50, J4, JP1 | Layers: B.Cu, In3.Cu, F.Cu

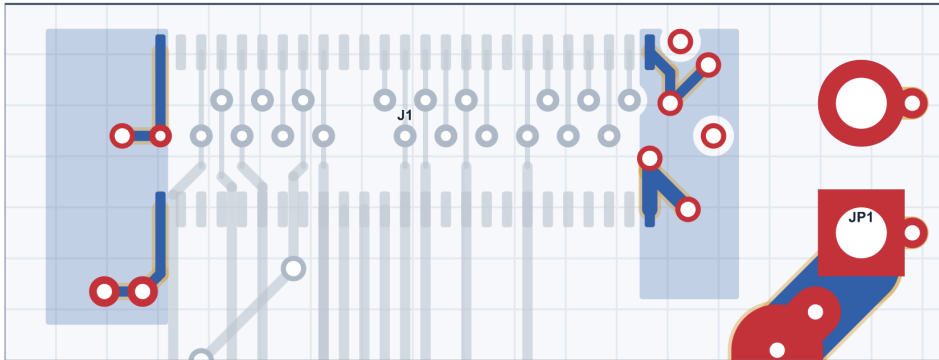
J1 supply and ground landings

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

J1 supply and ground landings
Example: BUCK_3V3 B.Cu 1.5 → 2.95 mm

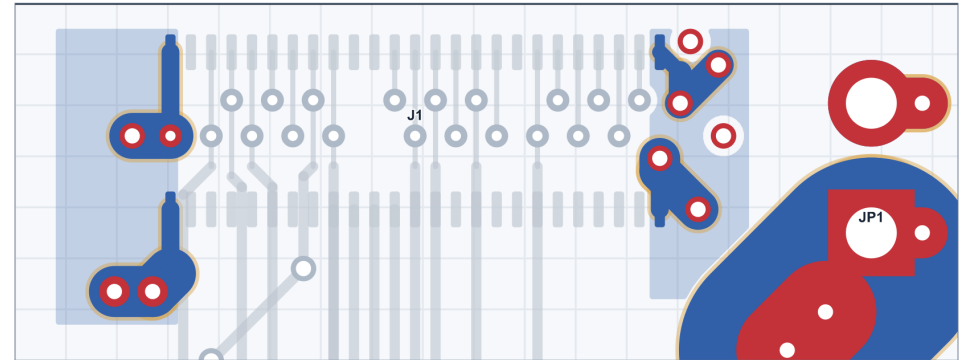


5 mm · exact same scale
B.Cu F.Cu changed width
Changed copper widths: 0.2, 0.3, 0.5, 1, 1.5, 1.8 mm · 19 native sections
Selected-net vias in window: 14 · changed tracks: 19 · top view; B.Cu not mirrored
Nets: BUCK_3V3, DGND, LDO_3V3

AFTER - R15

AFTER · R15

J1 supply and ground landings
Example: BUCK_3V3 B.Cu 1.5 → 2.95 mm



5 mm · exact same scale
B.Cu F.Cu changed width
Changed copper widths: 0.3–4.25 mm · 19 native sections
Selected-net vias in window: 14 · changed tracks: 19 · top view; B.Cu not mirrored
Nets: BUCK_3V3, DGND, LDO_3V3

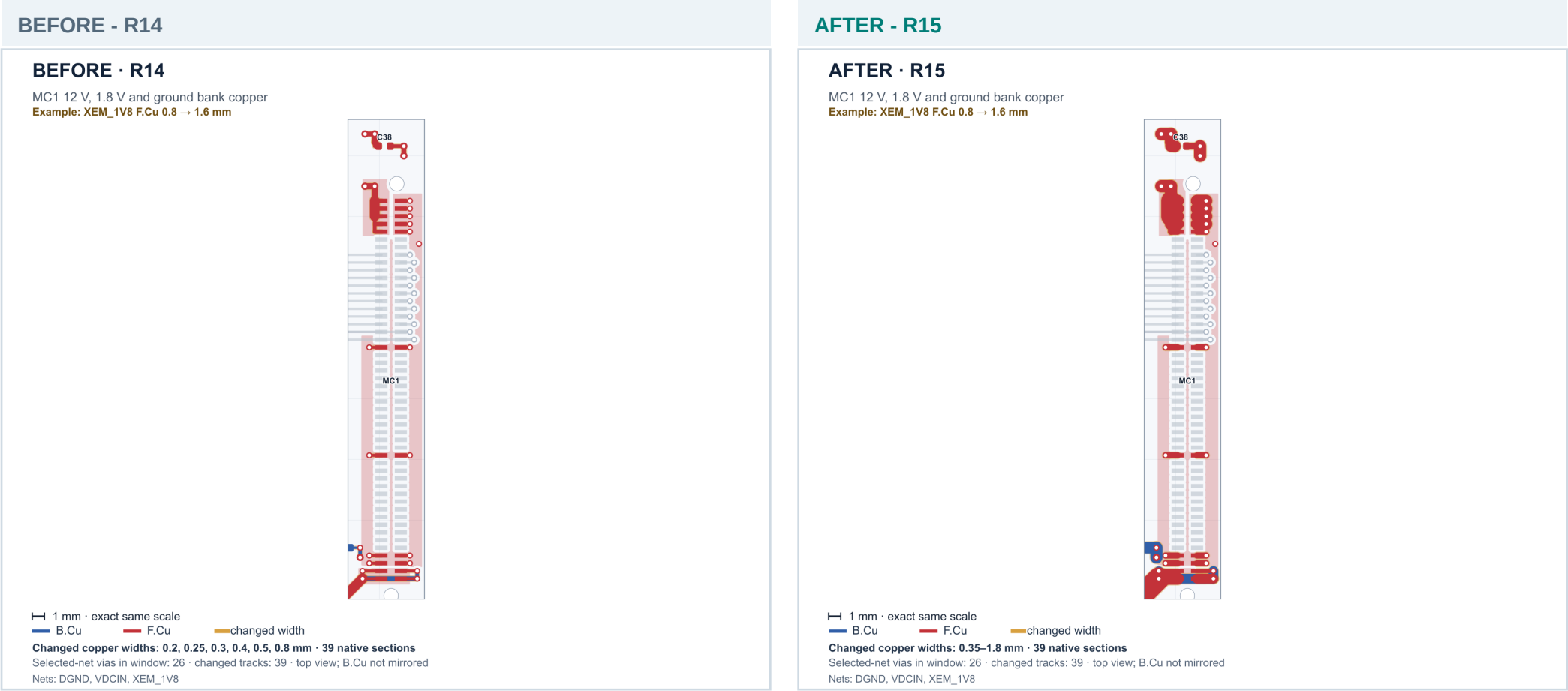
Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: J1, JP1 | Layers: B.Cu, F.Cu

MC1 12 V, 1.8 V and ground bank copper

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.



Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: MC1, C38 | Layers: B.Cu, F.Cu

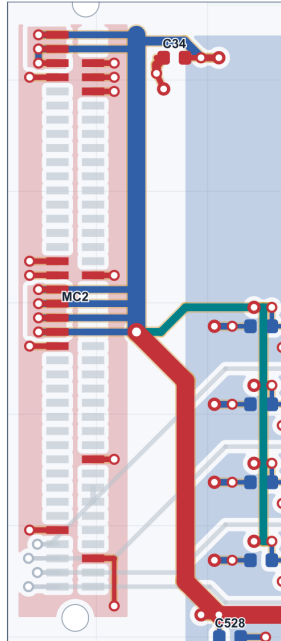
MC2 1.8 V and return copper

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

MC2 1.8 V and return copper
Example: XEM_1V8 F.Cu 0.8 → 2 mm

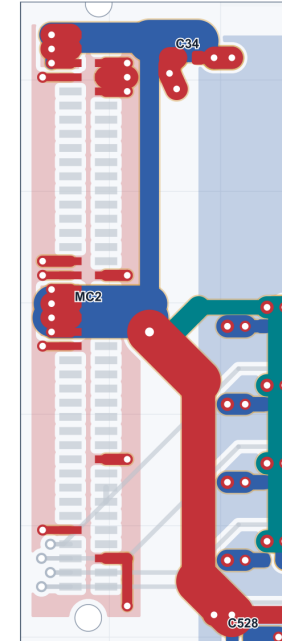


5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.2, 0.25, 0.3, 0.35, 0.4, 0.8 mm · 81 native sections
Selected-net vias in window: 46 · changed tracks: 81 · top view; B.Cu not mirrored
Nets: DGND, USBTAG_3V3, XEM_1V8

AFTER - R15

AFTER · R15

MC2 1.8 V and return copper
Example: XEM_1V8 F.Cu 0.8 → 2 mm



5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.35–2 mm · 81 native sections
Selected-net vias in window: 46 · changed tracks: 81 · top view; B.Cu not mirrored
Nets: DGND, USBTAG_3V3, XEM_1V8

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: MC2, C34, C528 | Layers: B.Cu, In3.Cu, F.Cu

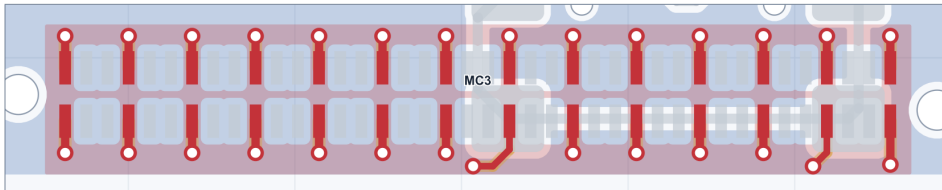
MC3 ground bank copper

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

MC3 ground bank copper
Example: DGND F.Cu 0.2 → 0.5 mm

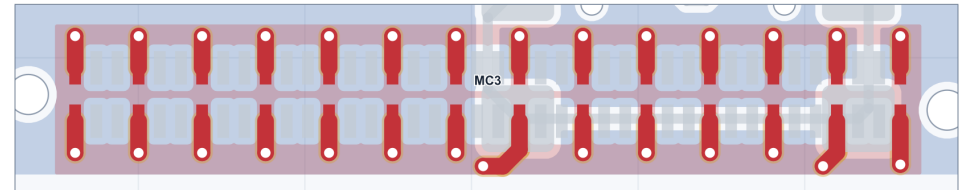


5 mm · exact same scale
B.Cu F.Cu changed width
Changed copper widths: 0.2, 0.25 mm · 31 native sections
Selected-net vias in window: 28 · changed tracks: 31 · top view; B.Cu not mirrored
Nets: DGND

AFTER - R15

AFTER · R15

MC3 ground bank copper
Example: DGND F.Cu 0.2 → 0.5 mm



5 mm · exact same scale
B.Cu F.Cu changed width
Changed copper widths: 0.5 mm · 31 native sections
Selected-net vias in window: 28 · changed tracks: 31 · top view; B.Cu not mirrored
Nets: DGND

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: MC3 | Layers: B.Cu, F.Cu

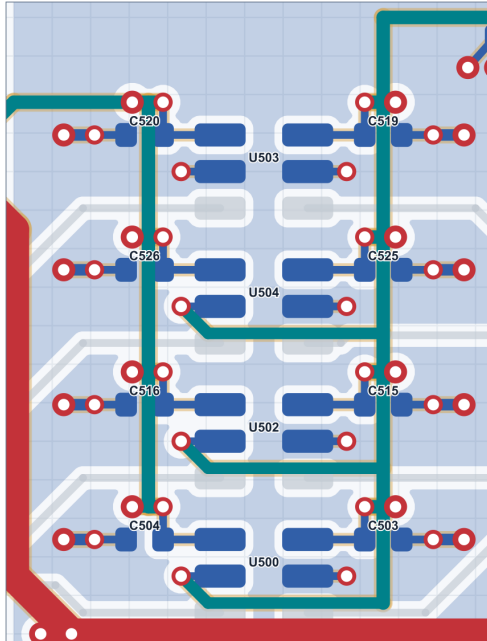
Four JTAG translator supply and bypass circuits

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

Four JTAG translator supply and bypass circuits
Example: USBJTAG_3V3 B.Cu 0.2 → 0.95 mm

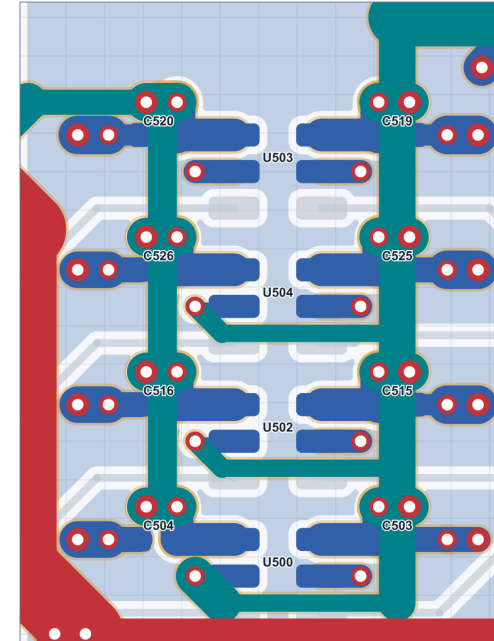


5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.2, 0.3, 0.35, 0.4, 0.8 mm · 80 native sections
Selected-net vias in window: 43 · changed tracks: 80 · top view; B.Cu not mirrored
Nets: DGND, USBJTAG_3V3, XEM_1V8

AFTER - R15

AFTER · R15

Four JTAG translator supply and bypass circuits
Example: USBJTAG_3V3 B.Cu 0.2 → 0.95 mm



5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.45–2 mm · 80 native sections
Selected-net vias in window: 43 · changed tracks: 80 · top view; B.Cu not mirrored
Nets: DGND, USBJTAG_3V3, XEM_1V8

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: U500, U502, U503, U504, C503, C504, C515, C516, C519, C520, C525, C526 | Layers: B.Cu, In3.Cu, F.Cu

FTDI core and left-side supply/bypass copper

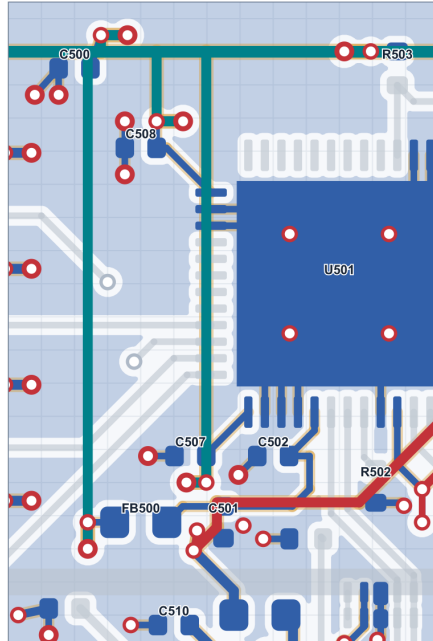
Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

FTDI core and left-side supply/bypass copper

Example: DGNB B.Cu 0.2 → 1 mm



5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width

Changed copper widths: 0.2, 0.25, 0.3, 0.35 mm · 80 native sections

Selected-net vias in window: 35 · changed tracks: 80 · top view; B.Cu not mirrored

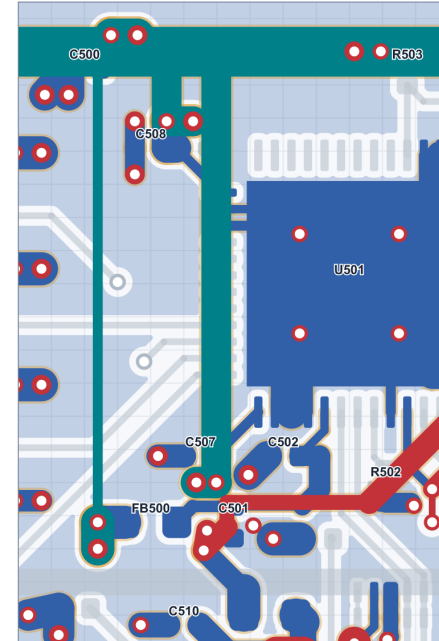
Nets: DGNB, USBJTAG_3V3, USBJTAG_VBUS_C, USBJTAG_VPHY, USBJTAG_VPLL, USBJTAG_VREGIN

AFTER - R15

AFTER · R15

FTDI core and left-side supply/bypass copper

Example: DGNB B.Cu 0.2 → 1 mm



5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width

Changed copper widths: 0.25–1.5 mm · 80 native sections

Selected-net vias in window: 35 · changed tracks: 80 · top view; B.Cu not mirrored

Nets: DGNB, USBJTAG_3V3, USBJTAG_VBUS_C, USBJTAG_VPHY, USBJTAG_VPLL, USBJTAG_VREGIN

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: U501, C500, C501, C502, C507, C510, FB500, R502, R503 | Layers: B.Cu, In3.Cu, F.Cu

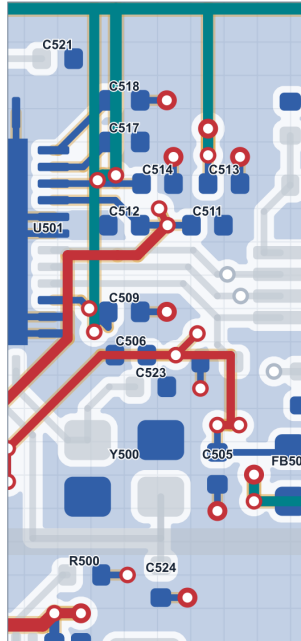
FTDI right-side filtered rails and returns

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

FTDI right-side filtered rails and returns
Example: USBJTAG_VPHY B.Cu 0.2 → 1 mm



1 mm · exact same scale
B.Cu In3.Cu F.Cu

changed width

Changed copper widths: 0.2, 0.25, 0.3, 0.35, 0.4 mm · 69 native sections

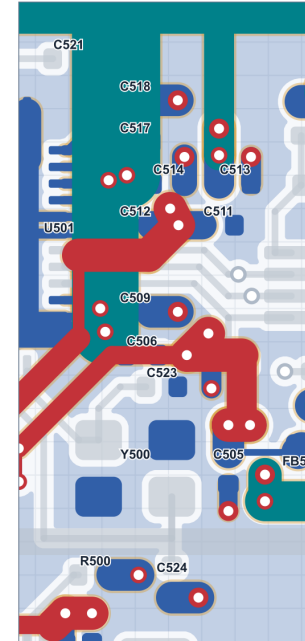
Selected-net vias in window: 26 · changed tracks: 69 · top view; B.Cu not mirrored

Nets: DGND, USBJTAG_3V3, USBJTAG_VBUS_C, USBJTAG_VCCA, USBJTAG_VCORE, USBJTAG_VPHY, USBJTAG_VREGIN

AFTER - R15

AFTER · R15

FTDI right-side filtered rails and returns
Example: USBJTAG_VPHY B.Cu 0.2 → 1 mm



1 mm · exact same scale
B.Cu In3.Cu F.Cu

changed width

Changed copper widths: 0.25–2 mm · 69 native sections

Selected-net vias in window: 26 · changed tracks: 69 · top view; B.Cu not mirrored

Nets: DGND, USBJTAG_3V3, USBJTAG_VBUS_C, USBJTAG_VCCA, USBJTAG_VCORE, USBJTAG_VPHY, USBJTAG_VREGIN

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: U501, C505, C506, C509, C511, C512, C513, C514, C517, C518, C521, C523, C524, Y500, R500, FB501 | Layers: B.Cu, In3.Cu, F.Cu

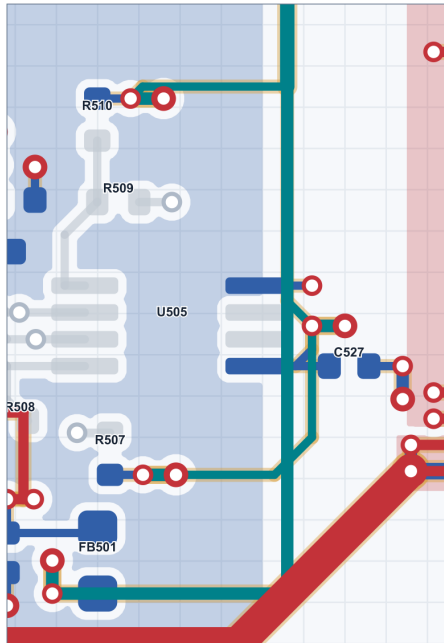
EEPROM and nearby 3.3 V branches

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

EEPROM and nearby 3.3 V branches
Example: USBTAG_3V3 B.Cu 0.2 → 1 mm

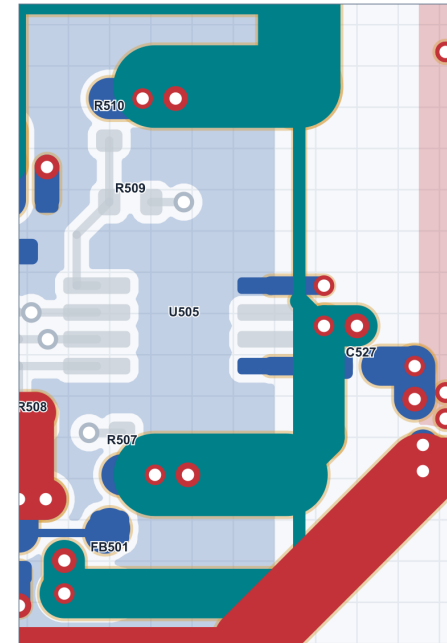


1 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.2, 0.25, 0.3, 0.35, 0.4, 0.8 mm · 44 native sections
Selected-net vias in window: 20 · changed tracks: 44 · top view; B.Cu not mirrored
Nets: DGND, USBTAG_3V3, USBTAG_VPHY, XEM_1V8

AFTER - R15

AFTER · R15

EEPROM and nearby 3.3 V branches
Example: USBTAG_3V3 B.Cu 0.2 → 1 mm



1 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.25–2 mm · 44 native sections
Selected-net vias in window: 20 · changed tracks: 44 · top view; B.Cu not mirrored
Nets: DGND, USBTAG_3V3, USBTAG_VPHY, XEM_1V8

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: U505, C527, R507, R508, R509, R510, FB501 | Layers: B.Cu, In3.Cu, F.Cu

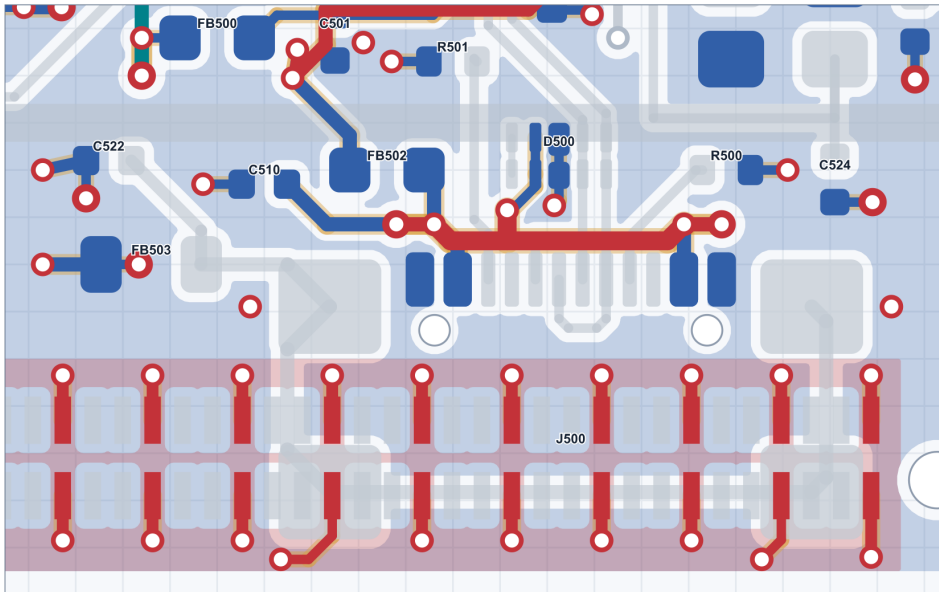
USB power, protection and filtered-shell returns

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

USB power, protection and filtered-shell returns
Example: USBJTAG_VREGIN B.Cu 0.3 → 1 mm

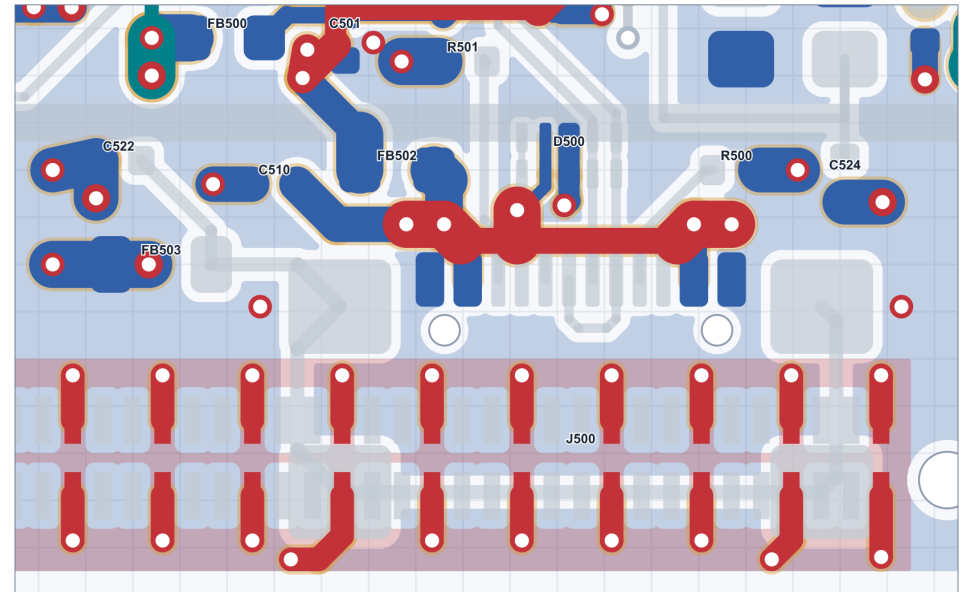


5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.2, 0.25, 0.3, 0.4 mm · 73 native sections
Selected-net vias in window: 45 · changed tracks: 73 · top view; B.Cu not mirrored
Nets: DGND, USBJTAG_3V3, USBJTAG_VBUS_C, USBJTAG_VPLL, USBJTAG_VREGIN

AFTER - R15

AFTER · R15

USB power, protection and filtered-shell returns
Example: USBJTAG_VREGIN B.Cu 0.3 → 1 mm



5 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.25–1 mm · 73 native sections
Selected-net vias in window: 45 · changed tracks: 73 · top view; B.Cu not mirrored
Nets: DGND, USBJTAG_3V3, USBJTAG_VBUS_C, USBJTAG_VPLL, USBJTAG_VREGIN

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: J500, D500, C501, C510, C522, C524, FB500, FB502, FB503, R500, R501 | Layers: B.Cu, In3.Cu, F.Cu

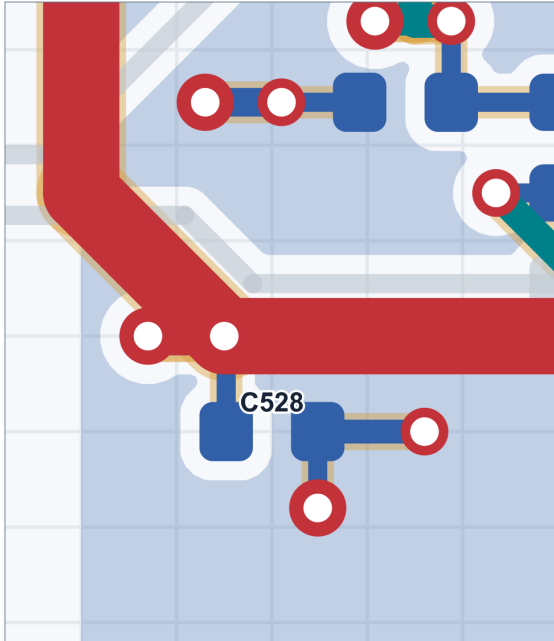
Far-end 1.8 V feed and C528 bypass

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

Far-end 1.8 V feed and C528 bypass
Example: XEM_1V8 F.Cu 0.4 → 1 mm



1 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.2, 0.25, 0.3, 0.35, 0.4, 0.8 mm · 17 native sections
Selected-net vias in window: 9 · changed tracks: 17 · top view; B.Cu not mirrored
Nets: DGND, USBJTAG_3V3, XEM_1V8

AFTER - R15

AFTER · R15

Far-end 1.8 V feed and C528 bypass
Example: XEM_1V8 F.Cu 0.4 → 1 mm



1 mm · exact same scale
B.Cu In3.Cu F.Cu changed width
Changed copper widths: 0.55–2 mm · 17 native sections
Selected-net vias in window: 9 · changed tracks: 17 · top view; B.Cu not mirrored
Nets: DGND, USBJTAG_3V3, XEM_1V8

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: C528 | Layers: B.Cu, In3.Cu, F.Cu

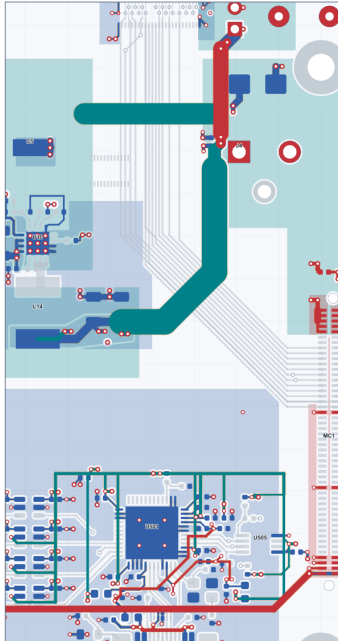
Rail distribution between local power blocks

Identical coordinates, crop, scale and copper layers. Both sides use actual native saved geometry and fills.

BEFORE - R14

BEFORE · R14

Rail distribution between local power blocks
Example: XEM_1V8 F.Cu 0.8 → 1.8 mm



10 mm · exact same scale
B.Cu In3.Cu F.Cu changed width

Changed copper widths: 0.2–3 mm · 342 native sections

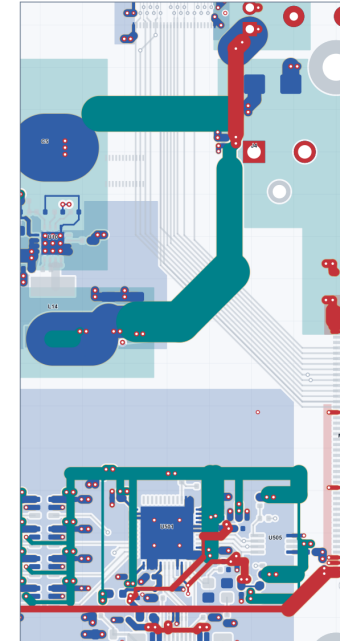
Selected-net vias in window: 164 · changed tracks: 342 · top view; B.Cu not mirrored

Nets: BUCK_3V3, DGND, LDO_3V3, USBJTAG_3V3, USBJTAG_VBUS_C, USBJTAG_VCCA, USBJTAG_VCORE, USBJTAG_VPHY, USBJTAG_...

AFTER - R15

AFTER · R15

Rail distribution between local power blocks
Example: XEM_1V8 F.Cu 0.8 → 1.8 mm



10 mm · exact same scale
B.Cu In3.Cu F.Cu changed width

Changed copper widths: 0.25–8 mm · 342 native sections

Selected-net vias in window: 164 · changed tracks: 342 · top view; B.Cu not mirrored

Nets: BUCK_3V3, DGND, LDO_3V3, USBJTAG_3V3, USBJTAG_VBUS_C, USBJTAG_VCCA, USBJTAG_VCORE, USBJTAG_VPHY, USBJTAG_...

Native copper shows the actual widths before and after at the same physical extent, layer set and magnification. The header gives one exact local width change.

- Exact widths are listed in millimetres below. Native filled copper is shown; component placement, track centerlines and via positions are unchanged.
- Other copper is dimmed for clearance context. Reference labels and thin gold width markers are explanatory overlays; the markers may be subtle at overview scale.

Parts: J4, C5, U10, L14, MC1, U501, U505 | Layers: B.Cu, In3.Cu, F.Cu

Checks, retained narrow sections and source identity

Review the width ledger for every changed track and the native project for exact routing.

- Independent raw-file audit: all 81 footprints, 298 vias, 720 segment centerlines/endpoints, zone outlines/settings, six-layer stack, 53 x 83 mm outline and schematic electrical structure are unchanged. Only permitted existing track widths increase.
- Fresh native PCB check: zero physical violations, zero disconnected items and zero schematic-parity findings under the retained project settings. The independent graph verifies all 250 relevant pad records, including all 213 former multi-via pad paths. No formerly reachable outer-layer via or plated-pad path was lost.
- Sensitive converter switch/bootstrap/feedback and quiet signal-ground branches, USB/JTAG signal traces, and direction-control ties retain their intended geometry. Short pad escapes may stay narrower than open trunks.
- The two previously documented D500 ESD single-via groups remain exceptions. Via count and drill sizes are unchanged. This width revision does not establish operating current, temperature rise, ESD/EMI performance, USB/JTAG function or assembled mating.
- Inherited schematic ERC (210 unused-pin errors and 13 off-grid warnings) and four strict footprint-filter warnings remain. This is a static routing review candidate, not a fabrication release.

Frozen native sources

R14 PCB SHA256: 05fb81c4c75c09fef54e3d5384e75692f4dd2b78c029711a95bf3864875aa2f7

R15 PCB SHA256: 61e693734a11f87cc2719fc4030975bb590dee46df228db0d5de3316b03ea035