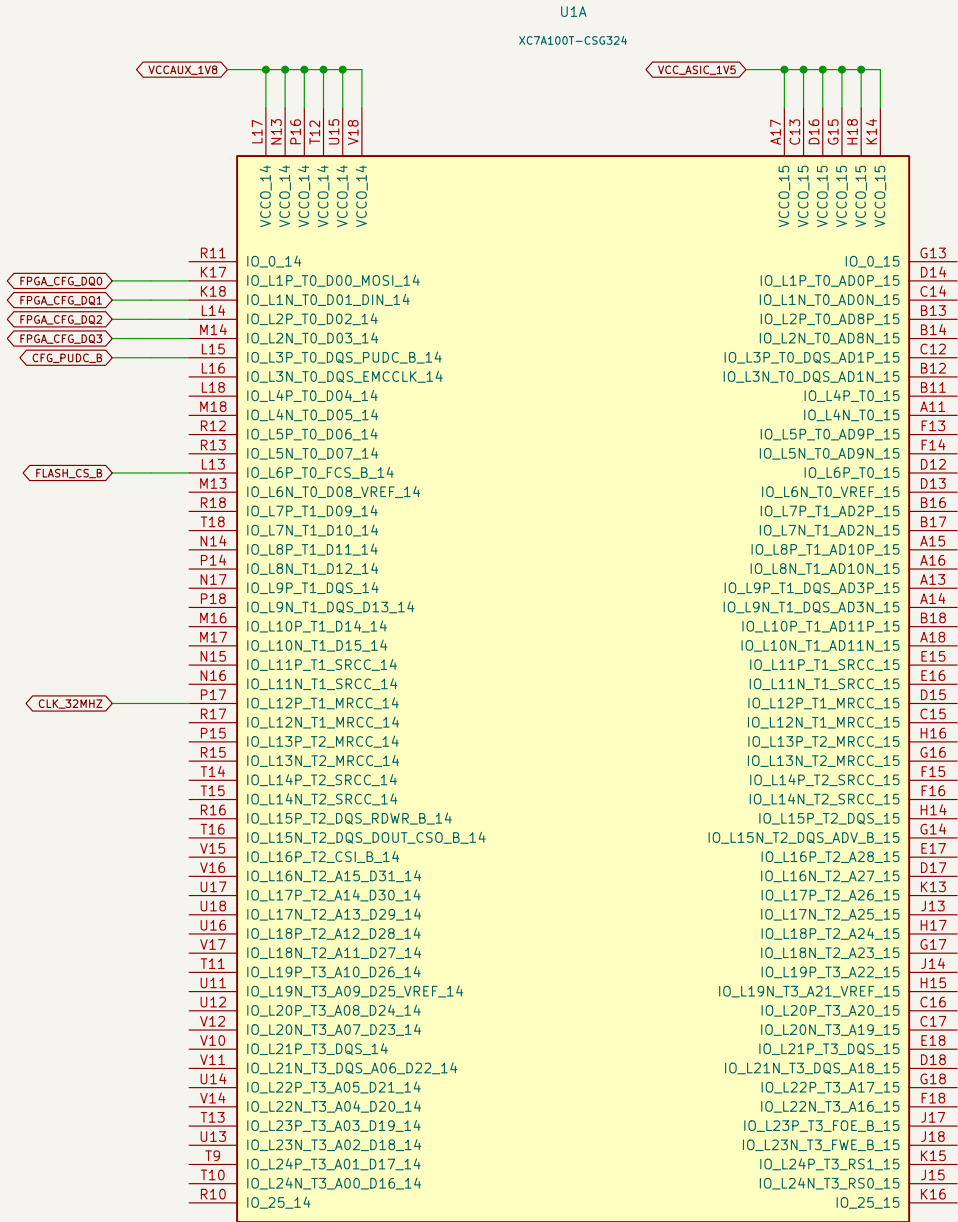


U1 / XC7A100T-CSG324 / I/O banks 14 and 15

15 x 15 mm CSG324. Unassigned I/O pins are deliberately open. The 117-signal ASIC interface is a confirmed budget; physical ASIC and receiver assignments remain deferred.



ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /U1 banks 14 and 15/

File: fpga_unit_01.kicad_sch

Title: U1 / XC7A100T-CSG324 / I/O banks 14 and 15

Size: A3

Date: 2026-09-26

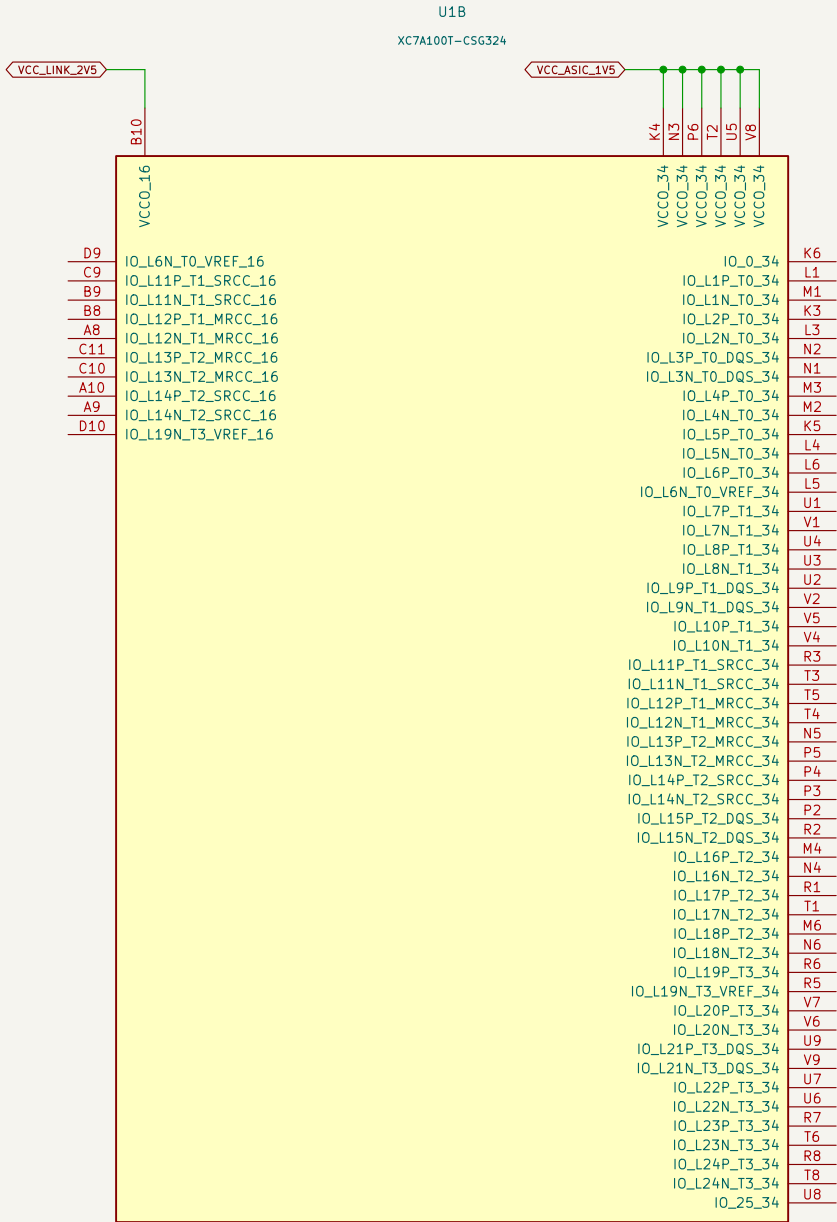
Rev: DEV 0.4

KiCad E.D.A. 10.0.6

Id: 2/20

U1 / XC7A100T-CSG324 / I/O banks 16 and 34

15 x 15 mm CSG324. Unassigned I/O pins are deliberately open. The 117-signal ASIC interface is a confirmed budget; physical ASIC and receiver assignments remain deferred.



ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /U1 banks 16 and 34/

File: fpga_unit_02.kicad_sch

Title: U1 / XC7A100T-CSG324 / I/O banks 16 and 34

Size: A3

Date: 2026-09-26

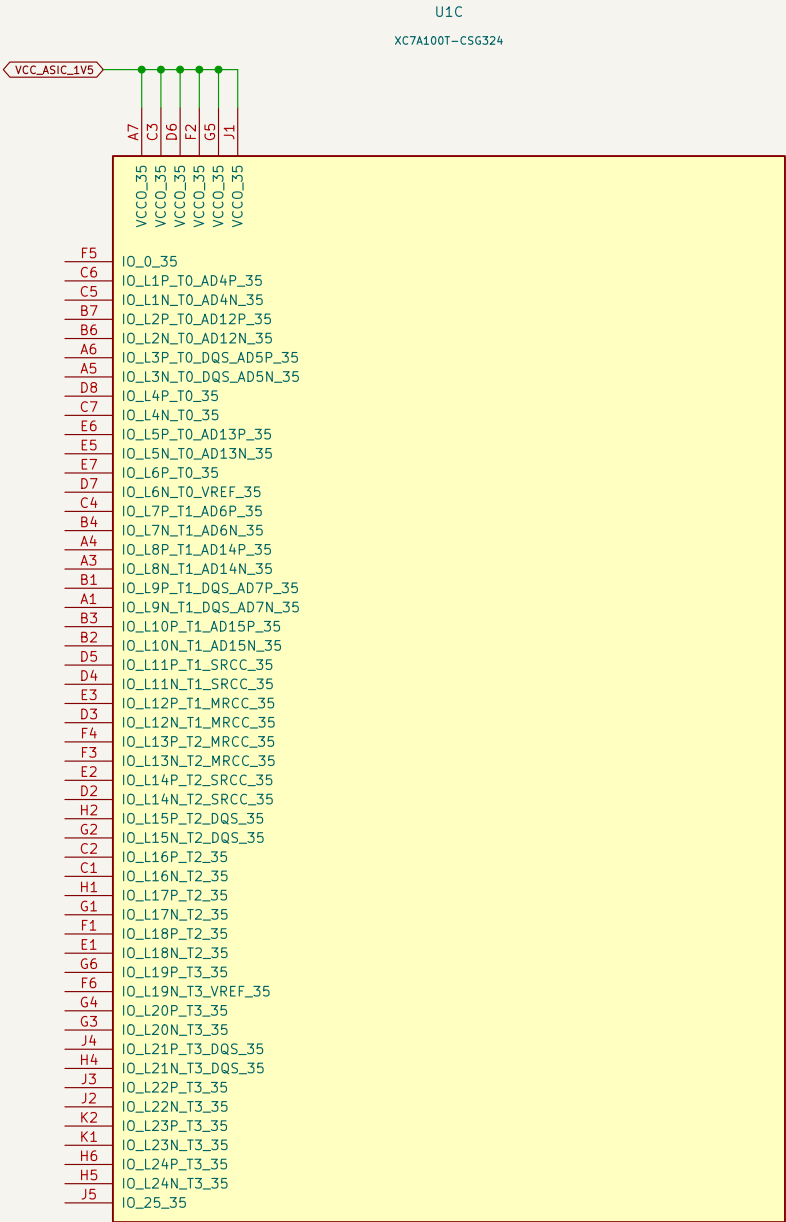
Rev: DEV 0.4

KiCad E.D.A. 10.0.6

Id: 3/20

U1 / XC7A100T-CSG324 / I/O bank 35

15 x 15 mm CSG324. Unassigned I/O pins are deliberately open. The 117-signal ASIC interface is a confirmed budget; physical ASIC and receiver assignments remain deferred.



ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /U1 bank 35/

File: fpga_unit_03.kicad_sch

Title: U1 / XC7A100T-CSG324 / I/O bank 35

Size: A3

Date: 2026-09-26

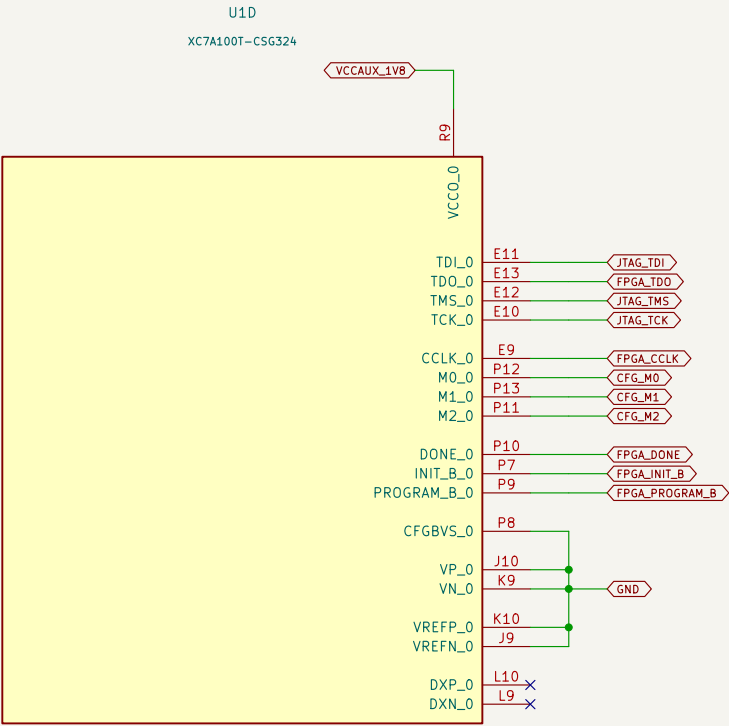
Rev: DEV 0.4

KiCad E.D.A. 10.0.6

Id: 4/20

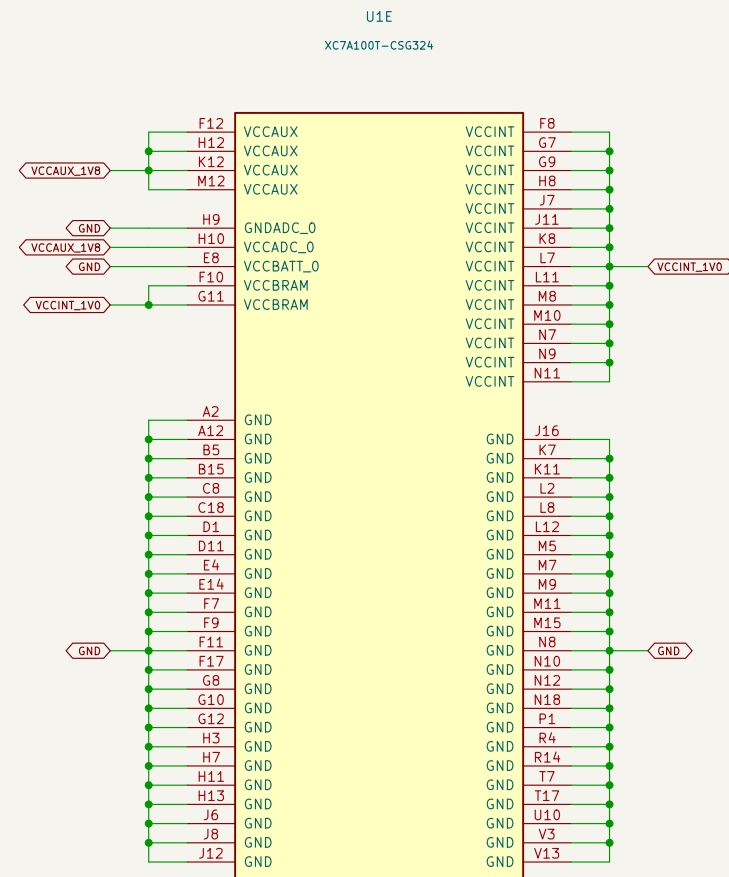
U1 / XC7A100T-CSG324 / Configuration, JTAG and analog support

15 x 15 mm CSG324. Unassigned I/O pins are deliberately open. The 117-signal ASIC interface is a confirmed budget; physical ASIC and receiver assignments remain deferred.



U1 / XC7A100T-CSG324 / Core, auxiliary power and ground

15 x 15 mm CSG324. Unassigned I/O pins are deliberately open. The 117-signal ASIC interface is a confirmed budget; physical ASIC and receiver assignments remain deferred.



ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /U1 core, auxiliary and ground/

File: fpga_unit_05.kicad_sch

Title: U1 / XC7A100T-CSG324 / Core, auxiliary power...

Size: A3

Date: 2026-09-26

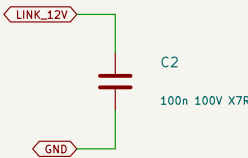
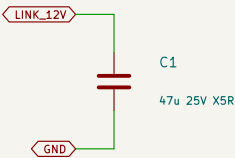
Rev: DEV 0.4

KiCad E.D.A. 10.0.6

id: 6/20

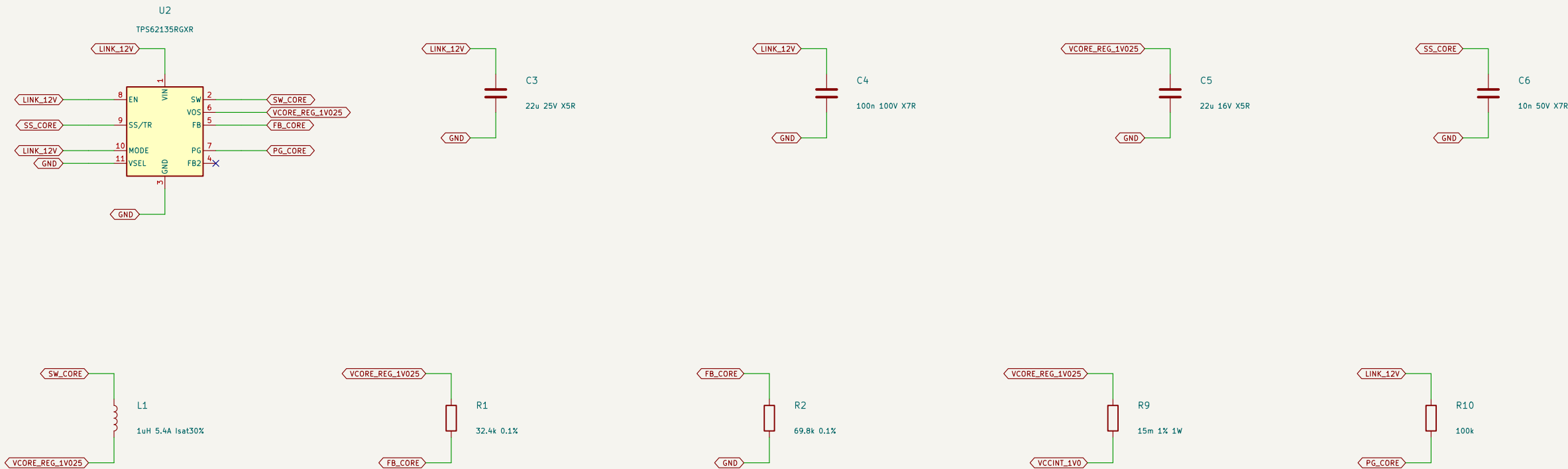
Cable input capacitors

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.



Core regulator / 1.0 V

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.



ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /Core regulator / 1.0 V/
File: core_02_01.kicad_sch

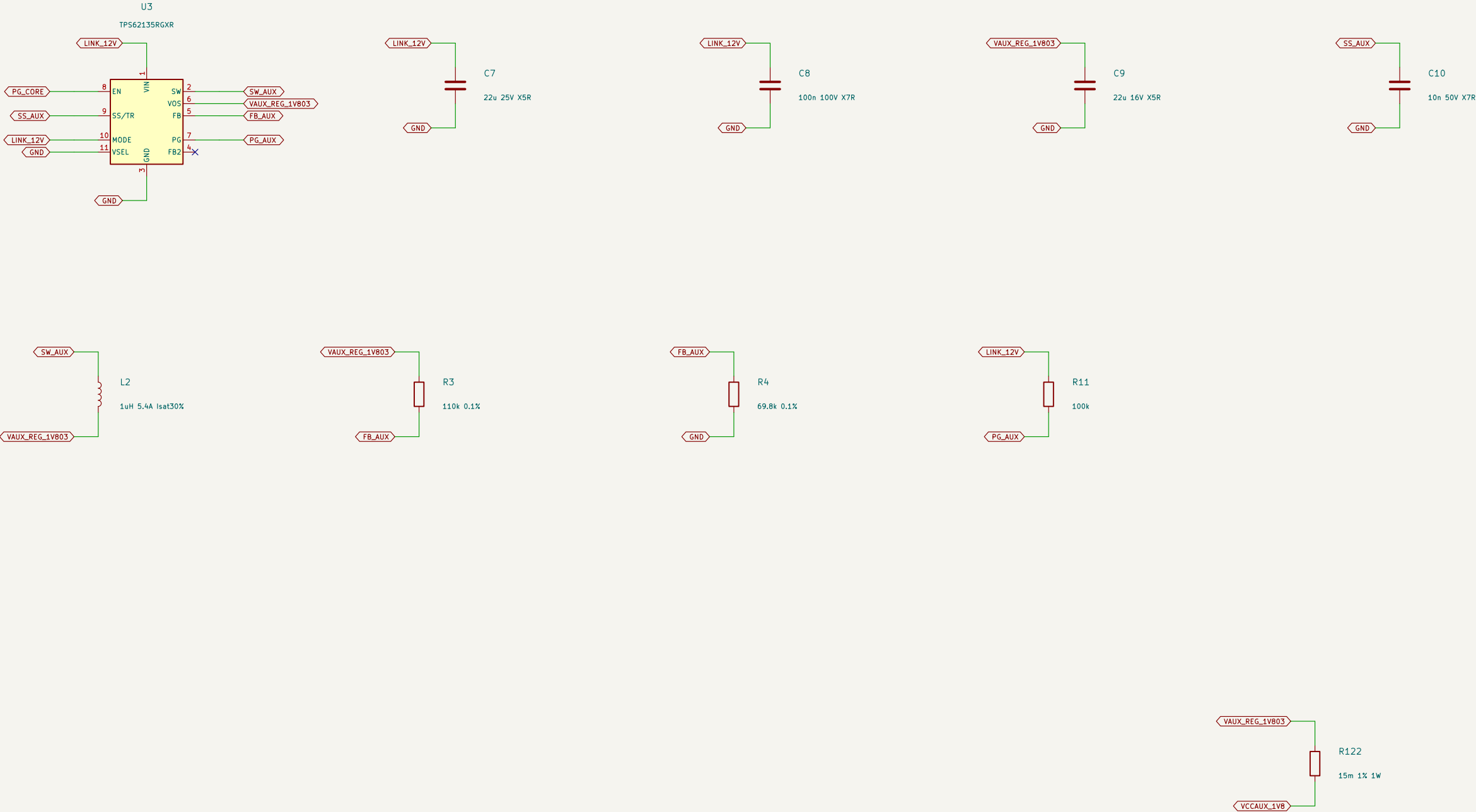
Title: Core regulator / 1.0 V

Size: A3
Date: 2026-09-26
KiCad E.D.A. 10.0.6

Rev: DEV 0.4
Id: 8/20

Auxiliary regulator / 1.8 V

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.



ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /Auxiliary regulator / 1.8 V/

File: core_03_01.kicad_sch

Title: Auxiliary regulator / 1.8 V

Size: A3

Date: 2026-09-26

Rev: DEV 0.4

KiCad E.D.A. 10.0.6

Id: 9/20

Bank16 link regulator / 2.5 V

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.

A

B

C

D

E

F

A

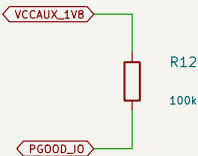
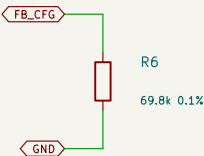
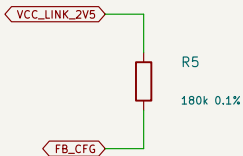
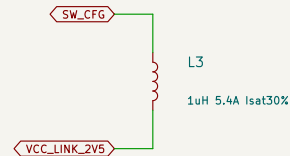
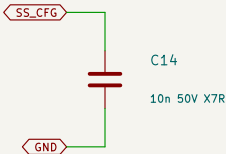
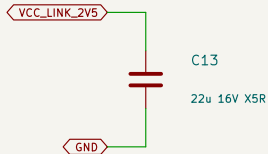
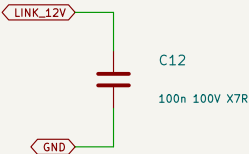
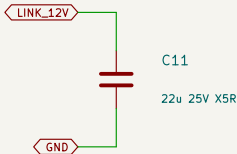
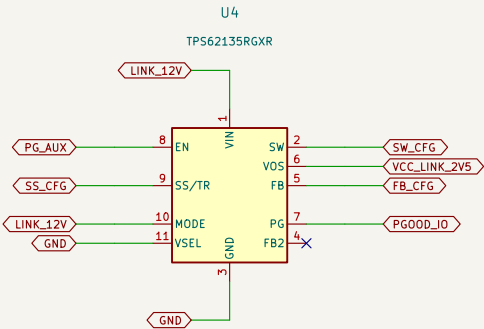
B

C

D

E

F



ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /Bank16 link regulator / 2.5 V/

File: core_04_01.kicad_sch

Title: Bank16 link regulator / 2.5 V

Size: A3

Date: 2026-09-26

Rev: DEV 0.4

KiCad E.D.A. 10.0.6

Id: 10/20

ASIC bank regulator / 1.5 V

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.

A

B

C

D

E

F

A

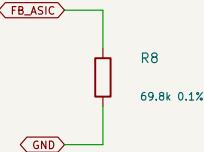
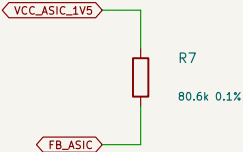
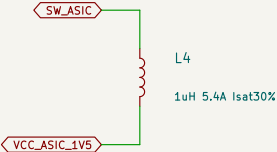
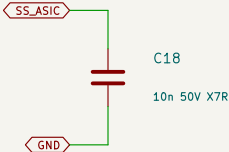
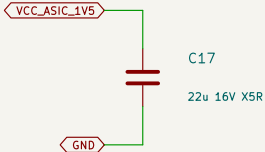
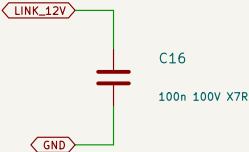
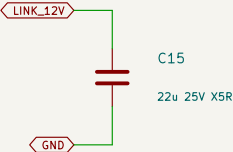
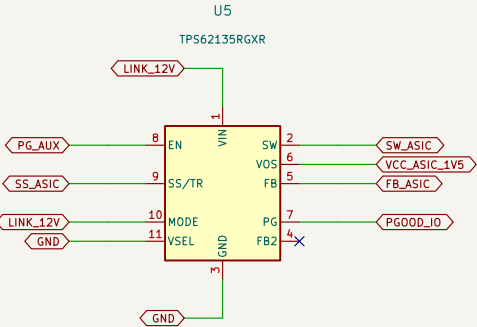
B

C

D

E

F



ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /ASIC bank regulator / 1.5 V/

File: core_05_01.kicad_sch

Title: ASIC bank regulator / 1.5 V

Size: A3

Date: 2026-09-26

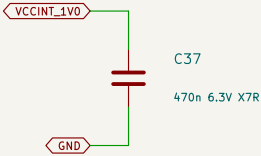
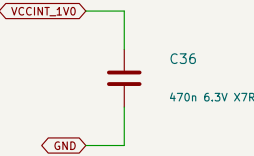
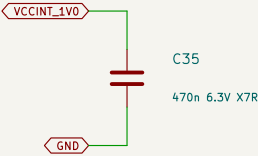
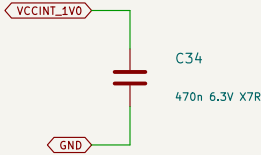
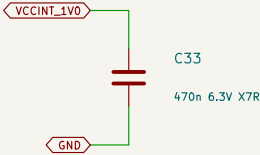
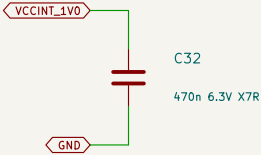
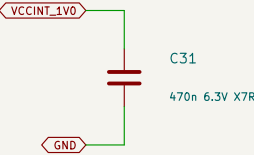
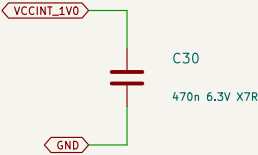
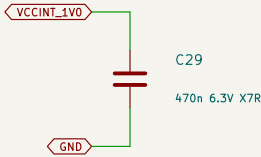
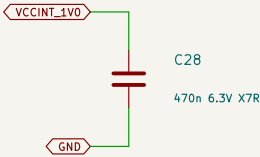
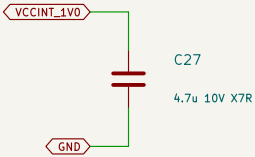
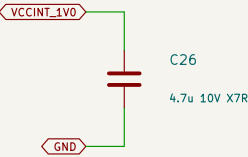
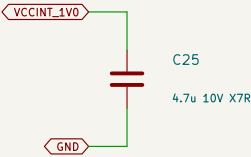
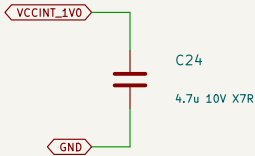
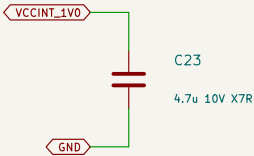
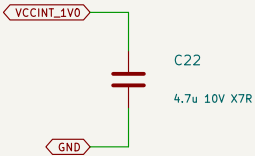
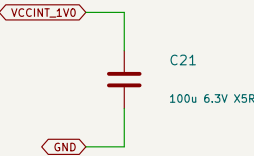
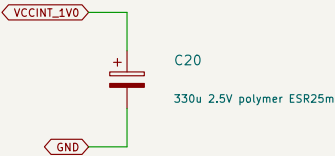
Rev: DEV 0.4

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Id: 11/20

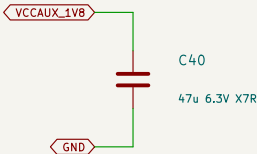
Decoupling / core and BRAM / 1.0 V

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.

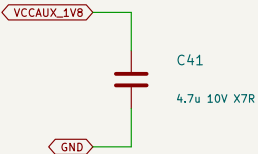


Decoupling / auxiliary and XADC / 1.8 V

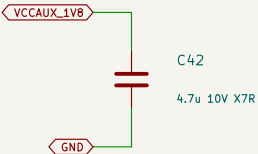
Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.



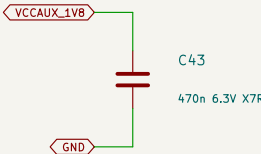
C40
47u 6.3V X7R



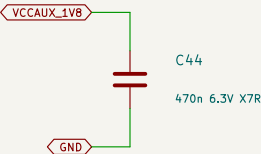
C41
4.7u 10V X7R



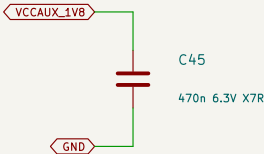
C42
4.7u 10V X7R



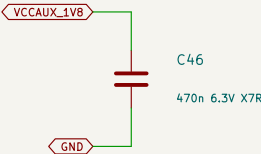
C43
470n 6.3V X7R



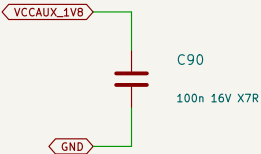
C44
470n 6.3V X7R



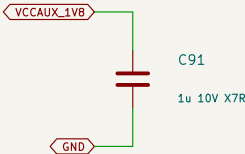
C45
470n 6.3V X7R



C46
470n 6.3V X7R



C90
100n 16V X7R



C91
1u 10V X7R

ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /Decoupling / auxiliary and XADC / 1.8 V/
File: core_07_01.kicad_sch

Title: Decoupling / auxiliary and XADC / 1.8 V

Size: A3
KiCad E.D.A. 10.0.6

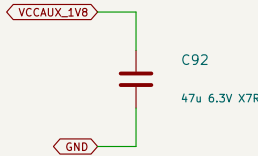
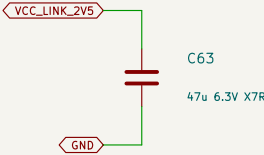
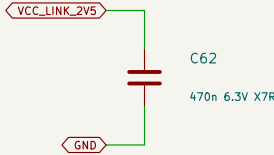
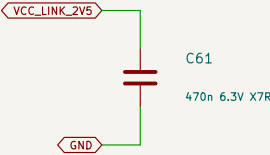
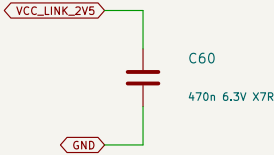
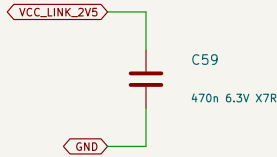
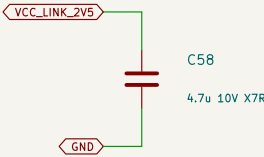
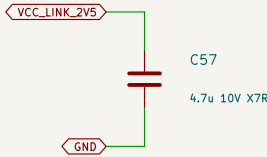
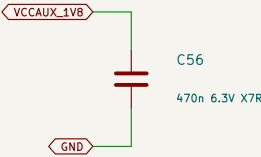
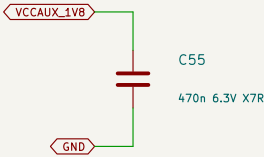
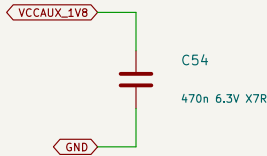
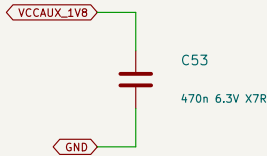
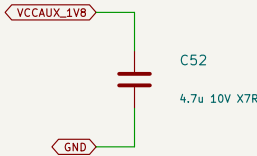
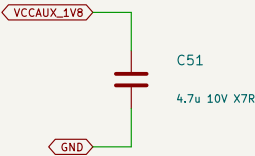
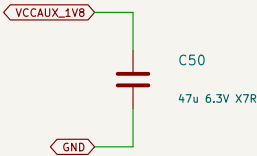
Date: 2026-09-26

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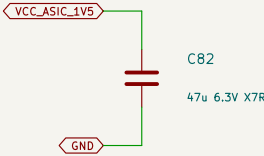
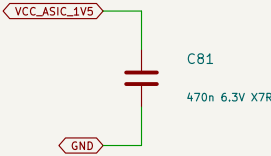
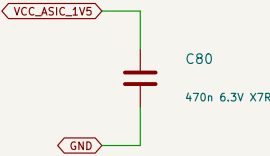
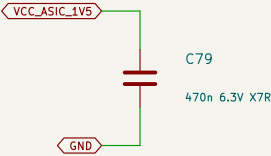
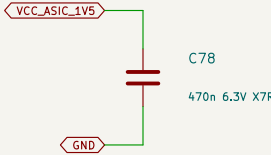
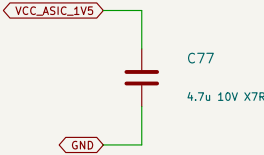
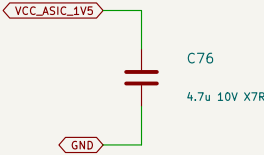
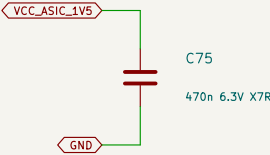
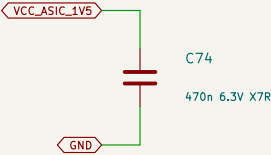
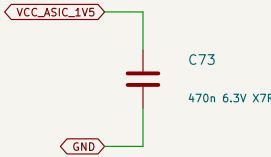
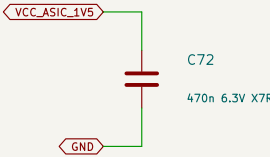
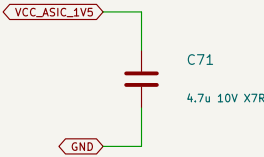
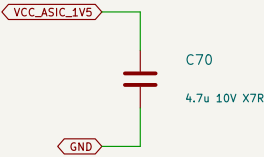
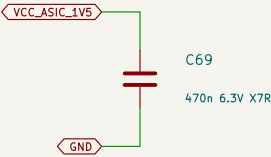
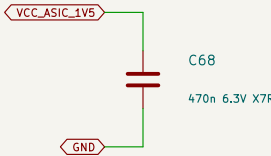
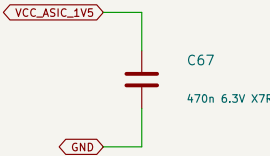
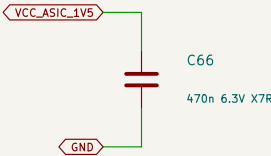
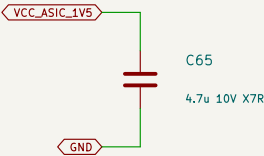
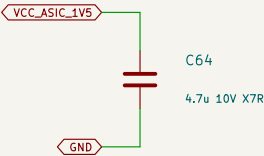
Decoupling / config1.8V and link2.5V

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.



Decoupling / ASIC-facing banks / 1.5 V

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.



ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /Decoupling / ASIC-facing banks / 1.5 V/
File: core_09_01.kicad_sch

Title: Decoupling / ASIC-facing banks / 1.5 V

Size: A3 Date: 2026-09-26

KiCad E.D.A. 10.0.6

Rev: DEV 0.4

Id: 15/20

Boot flash

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.

A

B

C

D

E

F

A

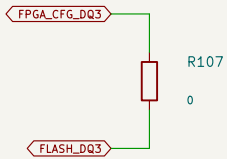
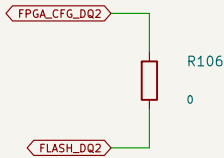
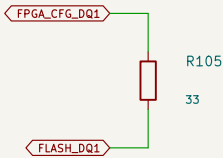
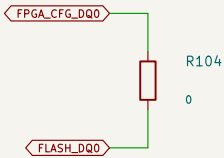
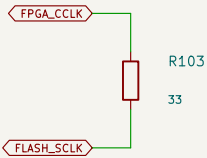
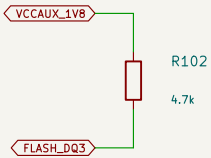
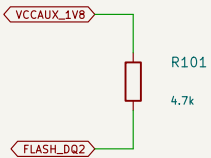
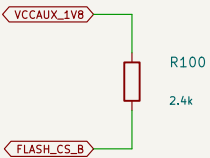
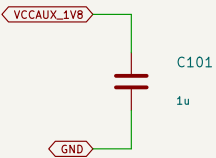
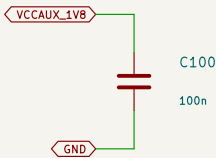
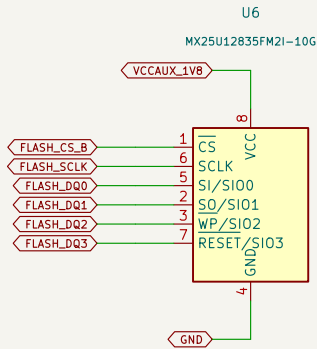
B

C

D

E

F



ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /Boot flash/
File: core_10_01.kicad_sch

Title: Boot flash

Size: A3 Date: 2026-09-26

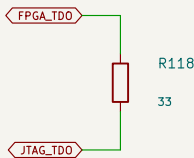
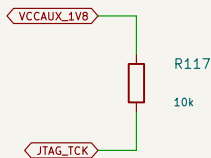
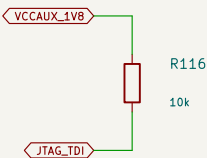
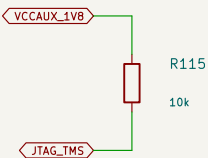
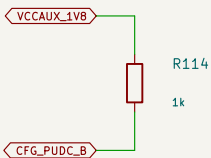
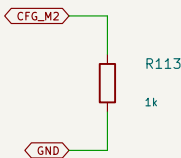
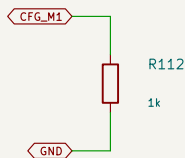
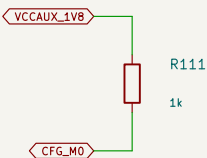
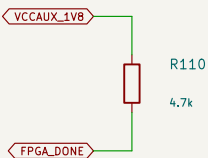
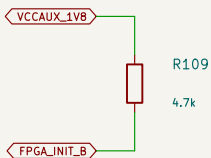
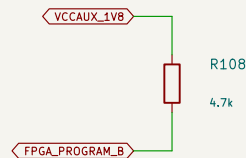
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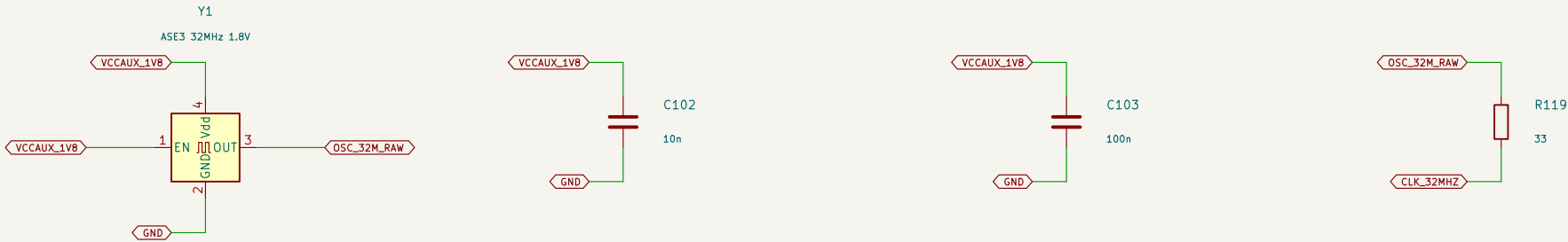
Programming JTAG

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.



Reference clock

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.



ENGINEERING DRAFT – NOT FOR FABRICATION

Howard Wang / XC7A100T CSG324

Sheet: /Reference clock/
File: core_12_01.kicad_sch

Title: Reference clock

Size: A3

Date: 2026-09-26

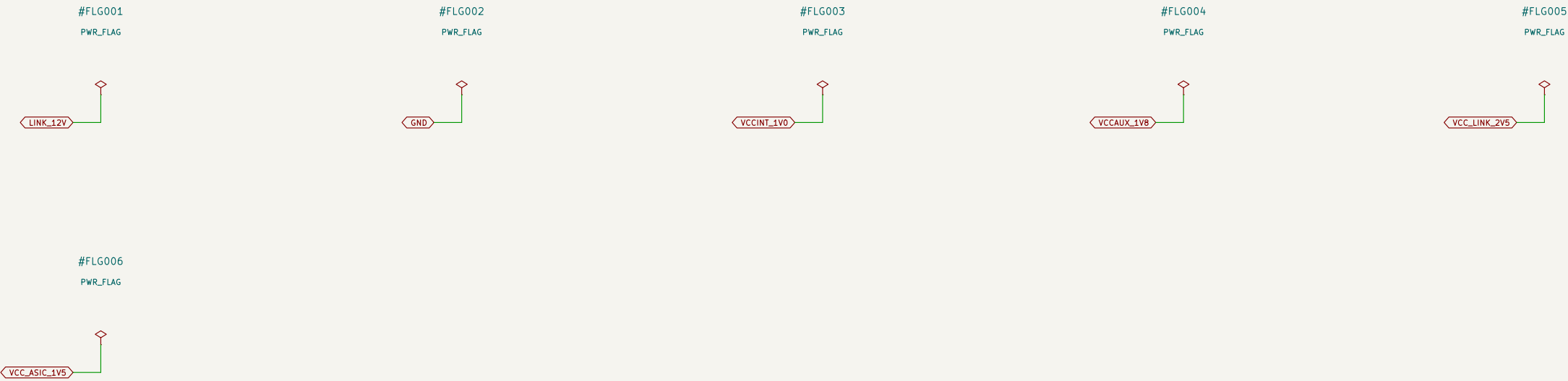
Rev: DEV 0.4

KiCad E.D.A. 10.0.6

Id: 18/20

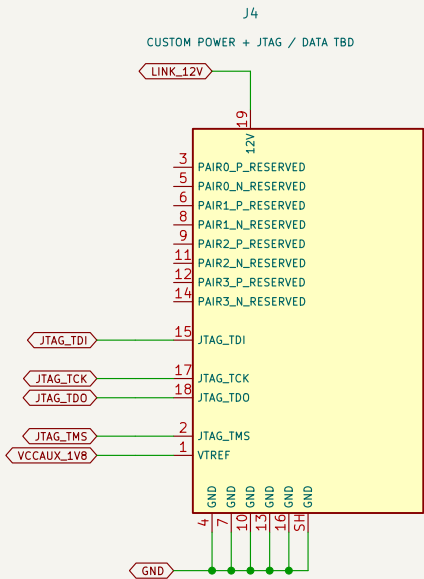
Power source assertions

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.



Custom shared cable / power and JTAG

Connected core draft. Matching global labels are electrical connections. Component status fields retain unresolved selections and requirements.



J4 / one custom cable connector

Contact	Net	Function
19	LINK_12V	Power input, proposed nominal 12 V
16	GND	DC return
1	VCC_LINK_2V5	Target voltage reference for programmer
2	JTAG_TMS	Programmer to FPGA E12
15	JTAG_TDI	Programmer to FPGA E11
17	JTAG_TCK	Programmer to FPGA E10
18	JTAG_TDO	FPGA E13 via R118 to programmer
4, 7, 10, 13, SH	GND	Pair shields and shell

Pins 3/5, 6/8, 9/11 and 12/14: reserved data pairs, not yet assigned.

12 V is a design proposal, not a qualified cable–power specification.

Requires a protected source and verified cable/contact current ratings.

Do not connect this custom–powered port to ordinary HDMI equipment.

No separate JTAG header, boot–mode jumper or test points.